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Near-field Mapping System to Scan in Time Domain the Magnetic Emissions of Integrated Circuits

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Abstract:

This paper introduces a low cost near-field mapping system. This system scans automatically and dynamically, in the time domain, the magnetic field emitted by integrated circuits during the execution of a repetitive set of instructions. Application of this measurement system is given to an industrial chip designed with a 180nm CMOS process. This application demonstrates the efficiency of the system but also the helpfulness of the results obtained to identify paths followed by the current and to locate the potential IR drop zones.

I-Introduction:

EM emissions observed on complex system on chip or system in package is often due to by switching currents of macro-functions or blocks integrated on silicon. In order to be able to model and simulate the EMI behavior of these complex circuits, the various sources of noise and their associated electrical paths should be identified and characterized.

However, characterizing the different source of noises and their associated electrical paths is an extremely difficult task while considering complex designs consisting of a several of macro-blocks such as RAM, ROM, FLASH, CPU, ADC, DAC, RF blocks, or analogue functions

Within this context, near-field measurement in time domain appears as an interesting solution to identify and characterize the various independent sources of EMI and their associated electrical paths within a chip. This is all the more interesting that performing a near-field scan in time domain allows identifying which operating scenario is the most critical from an EMC point of view but also detect at which time emissions are the strongest.

If some near field mapping systems have been reported to detect the high field level zones of integrated circuits, most of this previous works tackle the problem in the frequency domain [1,2,3,4]. Within this context, the main characteristic of the near-field scan mapping system is to deliver a fine resolution dynamic cartography of investigated chips.

The remainder of this paper is organized as follows. In section II, both the near-field mapping system and the mathematical treatment applied to the collected date are described. This system is then applied to a 180nm CMOS process testchip. Section III gives the results

obtained from the measures. Finally a conclusion is drawn section IV.

II-Measurement system

To analyze electromagnetic field radiated by the core of integrated circuits, a measurement platform has been developed.

a) Hardware

Figure 1 shows the different elements of the near-field scanner.

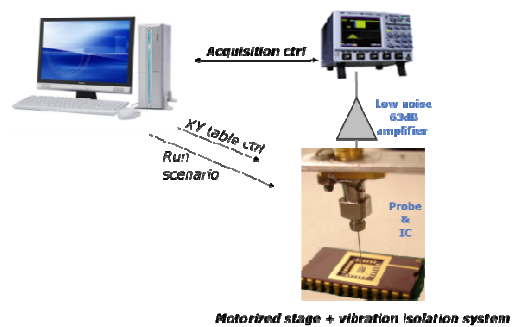


Fig. 1: Near-field scanner developed to measure the radiated field of IC core in the time domain

As shown, the Design Under Test (DUT) is controlled by a PC which sends a processing scenario, repeated during the entire measurement step, to the DUT via Ethernet or serial interfaces.

At the same time, the PC controls the the probe displacement via an XY table and stored the results of the measurements.

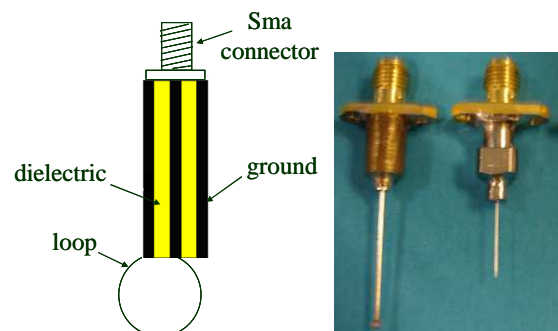


Fig. 22. 500µm and 40µm ØMagnetic probe

All probes used are passive with a bandwidth of 1.5 GHz. These probes are simple passive loops whose

diameter ranges from $50\mu\text{m}$ to $500\mu\text{m}$ that have been designed to be placed really close to the chip surface. Even if the magnetic probes are placed really close to the chip, the captured signal has low amplitude and need to be amplified. This is achieved, as shown figure 1, by a low noise 63db amplifier from MITEQ [6] connected to a 2GHz bandwidth Oscilloscope Waverunner 204Xi from LECROY [7] (which is controlled by the PC).

b) Acquisition method

To obtain the near-field scanning, a C script was developed to control the XY table. In this script, the displacement step in x and y are defined by the user; moreover x and y have to be initialized and bounded before running the full scan of the chip. To initialize and bound x and y values, the magnetic probe is first placed on a corner of the IC, and then place on the diagonally opposite corner. The area to be scanned being defined, the near-field scan starts with the wanted displacement step (from $100\mu\text{m}$ down to $10\mu\text{m}$).

For each x,y coordinate of the IC surface, the probe captures the evolution in time of the magnetic field once or many times in order to obtain a single shot waveform or an averaged one; the resulting waveforms are then store in the PC.

c) Post treatment of the measured data

Once all waveforms have been stored on the PC the post treatment of the data may start. Several post treatments are available.

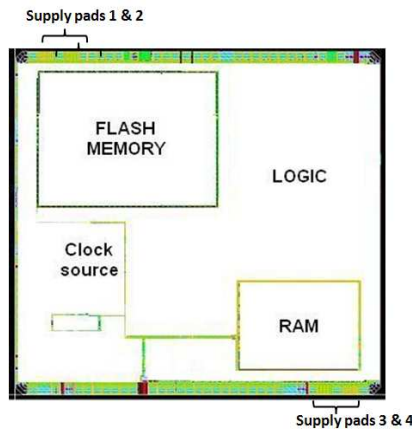


Fig. 3 Testchip floorplan

A first treatment can be applied to analyze the EMI in the frequency domain. It consists roughly of a Fast Fourier Transform (FFT), even if some scripts have been developed to analyze the power density on predefined frequency ranges.

A second treatment aims at computing the integral of the collected waveform in order to get a first order idea of the local switching current consumed by the chip.

Finally a last treatment may be applied to the collected data. It consists of making one picture of the EMI radiated by the chip for each measured sample of time. All these pictures are then gathered into a movie showing the evolution in time of the magnetic field over the full chip.

III-Experimental results

The near-field measurement system has been applied to an IC designed in a 180nm CMOS technology whose area is around 10mm^2 . This chip contains a CPU (denoted by logic in Figure 3), a FLASH, a RAM, and an internal clock generator delivering a 5.4MHz signal, and other small digital and analog blocks.

A processing scenario consisting of FLASH and RAM accesses (read and write) was stored in the FLASH of the chip whose floorplan is given Figure 3. Note that the supply is provided by four pads.

This processing scenario stored in the FLASH, we measured the EM emissions radiated by this chip running the aforementioned scenario using a $200\mu\text{m}$ probes and a $100\mu\text{m}$ displacement step. This measurement step took 10 hours.

a) Near-field Scans in frequency domain

The data collected, we performed an analysis of the magnetic field radiated by this chip in the frequency domain, using a spectrum analyzer rather than an oscilloscope for more accuracy. More precisely, we computed energy density map represented figures 4a and figure 4b the spectrums measured at x,y coordinates corresponding to the dots figure 4a. Note that the considered frequency range was [1MHz, 1 GHz].

As shown figure 4, the FLASH appears as the major source of electromagnetic emissions while the CPU, the RAM, and the clock generator have significantly lower emissions.

Despite these four functional blocks, the map also discloses a vertical bar whose emissions are significantly greater than those of the RAM, of the CPU and of the clock generator. Comparing the obtained map with the layout of the design, we identified this bar has a fraction of the supply rails close to the core supply pad. Note here that only this part of the supply rail was disclosed by the spectral analysis.

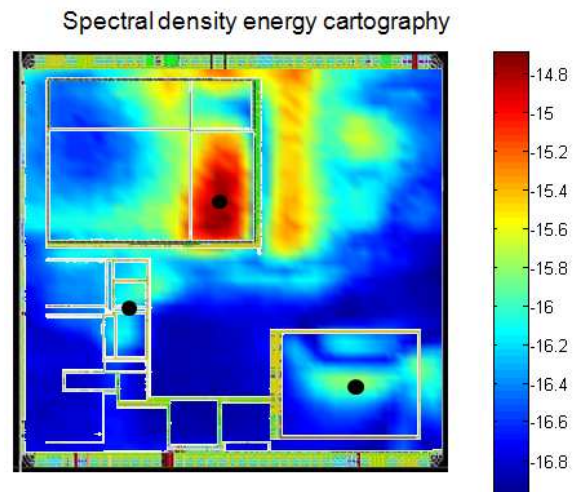


Fig. 4a Global spectral density energy cartography

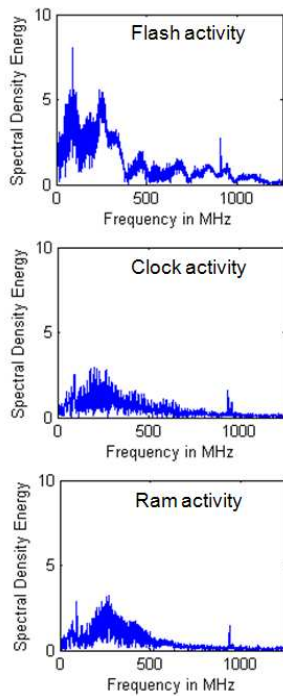


Fig. 5b Flash, Clock generator and RAM spectrum

b) Near-field Scans in time domain

In a second step, we elaborated the map of the chip electromagnetic emissions in the time domain. From this movie we deduced a first static map of the electromagnetic emissions of the chip represented figure 5.

More precisely, the maximum value of the EMI over several clock cycles has been reported, for each location, on this map. As shown, this map is quite different to that obtained in the frequency domain (figure 4). Indeed, it clearly appears that the CPU, the RAM could generate locally and at some specific times a magnetic field equivalent to the one generated by the FLASH.

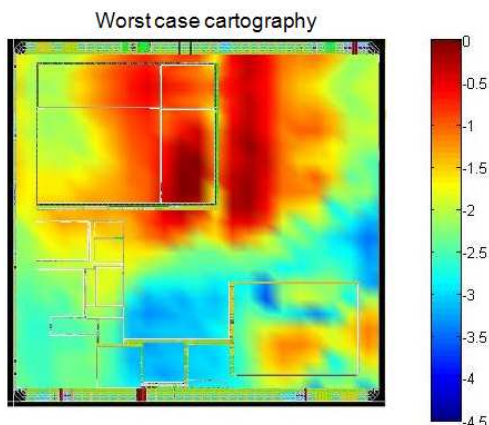


Fig. 6 Maximum magnetic field values map over several clock cycles

The identification of the time at which the RAM, and the CPU generate such important fields is easily done by looking to the movie that also disclose the electrical

paths followed by the switching current and also the potential hot spots from an IR drop point of view. As an illustration, figure 6a, 6b and 6c give some instantaneous maps of the magnetic field at three different times.

More precisely, Figure 6a gives the map while the CPU, the RAM and the FLASH are inactive. Figure 6b gives the map of the magnetic field while a data is read in the RAM, and finally figure 6c gives the map of the magnetic field while both the RAM and the FLASH are accessed (the executed code being stored in the FLASH).

With the knowledge of the floorplan and the power ground grid network of the chip it is then possible to deduce from the dynamic map (fig.6a 6c) the switching current flows in the chip for any specific instruction, and the related suspected IR drop zones.

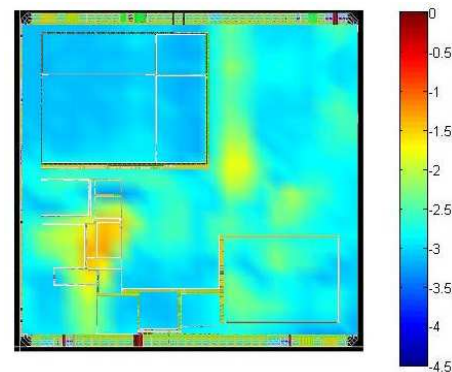


Fig. 6a Magnetic field map while only the clock generator is running

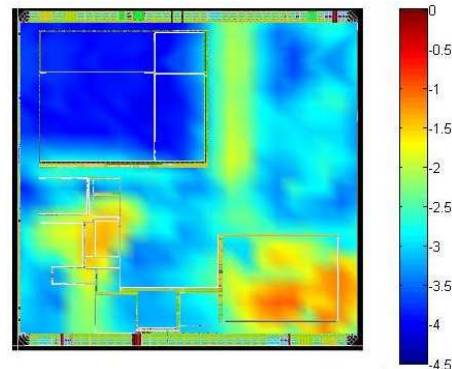


Fig. 6b Magnetic field map while a data is read in the RAM

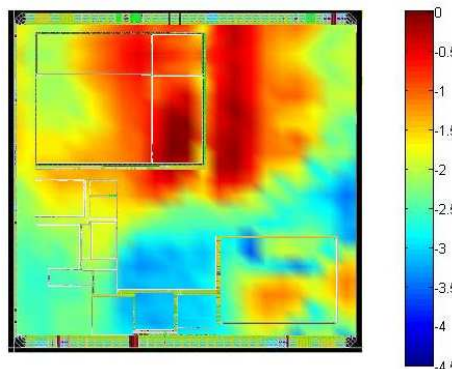
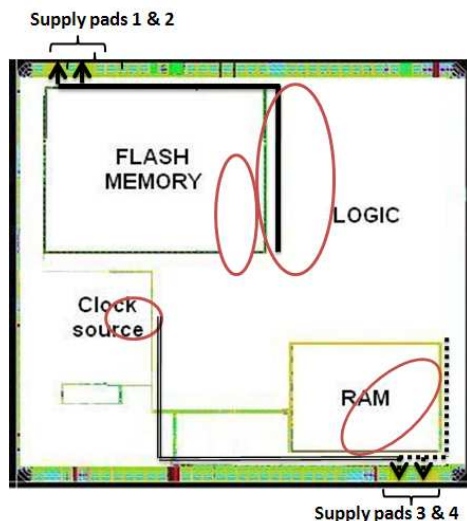


Fig. 6c Magnetic field map while the RAM and the EEPROM fire simultaneously

Proceeding as described for the clock generator we identified the different electrical paths followed by the switching currents. The identified paths are shown figure 8 as well as the related suspected IR drop zones.



c) Discussion

of a map (movie) obtained in the time domain. Comparing the results obtained, it appears that performing EME analyses in the time domain provides some interesting and complementary information that may be helpful in modeling the EMI radiated by VLSI cores.

IV-Conclusion

V- References

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